

therefore, line 2, line 6, line 10, line 14, . . . , line 1050, which define the "first even field". Next, signals representing lines 4, 8, 12, 16, . . . , 1048, are produced from A/D converter 118. In order to obtain all the even lines of the 1050 lines scanned by camera 12 in successive order, read/write controller 136 and address select circuit 134 operate to write each line of video information as output from even line buffer 124 in row address locations of the odd frame memory 128, according to the memory map of FIG. 8.

Specifically, during a first odd field time period, video information corresponding to line 2 is written in row address 001, line 6 in address 003, line 10 in address 005, . . . , line 1050 in address 525. That is, during the first even field time period, the video line information is written in successive odd row addresses of frame memory 128, as output from buffer 124.

During a second even field time period, video information corresponding to line 4 is written in row address 002, line 8 in address 004, line 12 in address 006, . . . , line 1048 in address 524. Accordingly, during the second even field time period, the video information is written in successive even row addresses of frame memory 128, as output from buffer 124.

The 525-line video information thus stored in even frame memory 128 defines, as shown in FIG. 8, consecutive even numbered lines of the 1050 line image frame to be reproduced by the receiving system.

Reproduction of the 1050 line high definition image is then carried out as follows.

Row addresses of the odd frame memory 126 are selected successively by address select circuit 130, in the order 001, 002, 003, . . . , 525, and the stored line information is read out and input to D/A converter stage 140.

Row addresses of the even frame memory 126 are selected successively by address select circuit 134, in the order 001, 002, 003, . . . , 525, and the stored line information is read out and input to D/A converter stage 142.

Outputs of the D/A converters 140, 142 are supplied to a high definition CRT drive system 146 for reproduction by a 1050 line CRT 148. It is presently contemplated that CRT 148 will be driven correspondingly to the camera 12 of the transmitting system. Namely, by use of a wobble signal generator or the like, adjacent pairs of lines, wherein each pair includes an odd and an even numbered line, are swept simultaneously across the CRT face.

Such an arrangement is disclosed in, for example, U.S. Patent 4,707,728.

C. Aural Transmission/Reception.

Audio signals may be frequency modulated in a conventional manner on one or both of the orthogonally polarized television signals radiated by the transmitting antennas 52, 56. Standard audio FM detector means in one or both of the tuner/demodulator systems 110, 112 then provides the detected audio to an amplifier and speaker system (not shown) associated with the receiving system.

Stereo sound can be realized by modulating, for example, a Left plus Right audio signal on one of the polarized transmitted signals, and a Left minus Right audio signal on the orthogonally polarized transmitted signal. When the demodulated audio signals are supplied to stereo FM decoding circuitry provided at the receiving system, separate Left and Right audio signals are obtained for amplification and sounding.

APPENDIX

- Figure 1 - Transmitter Configuration
- Figure 2 - Reception by Conventional Receivers
- Figure 3 - Propagation of Broadcast HDTV Signals
- Figure 4 - Receiving Set Configuration
- Figure 5 - Transmitter Memory Store - "Odd" Line Frames
- Figure 6 - Transmitter Memory Store - "Even" Line Frames
- Figure 7 - HDTV Receiver Memory Store - Odd Lines
- Figure 8 - HDTV Receiver Memory Store - Even Lines

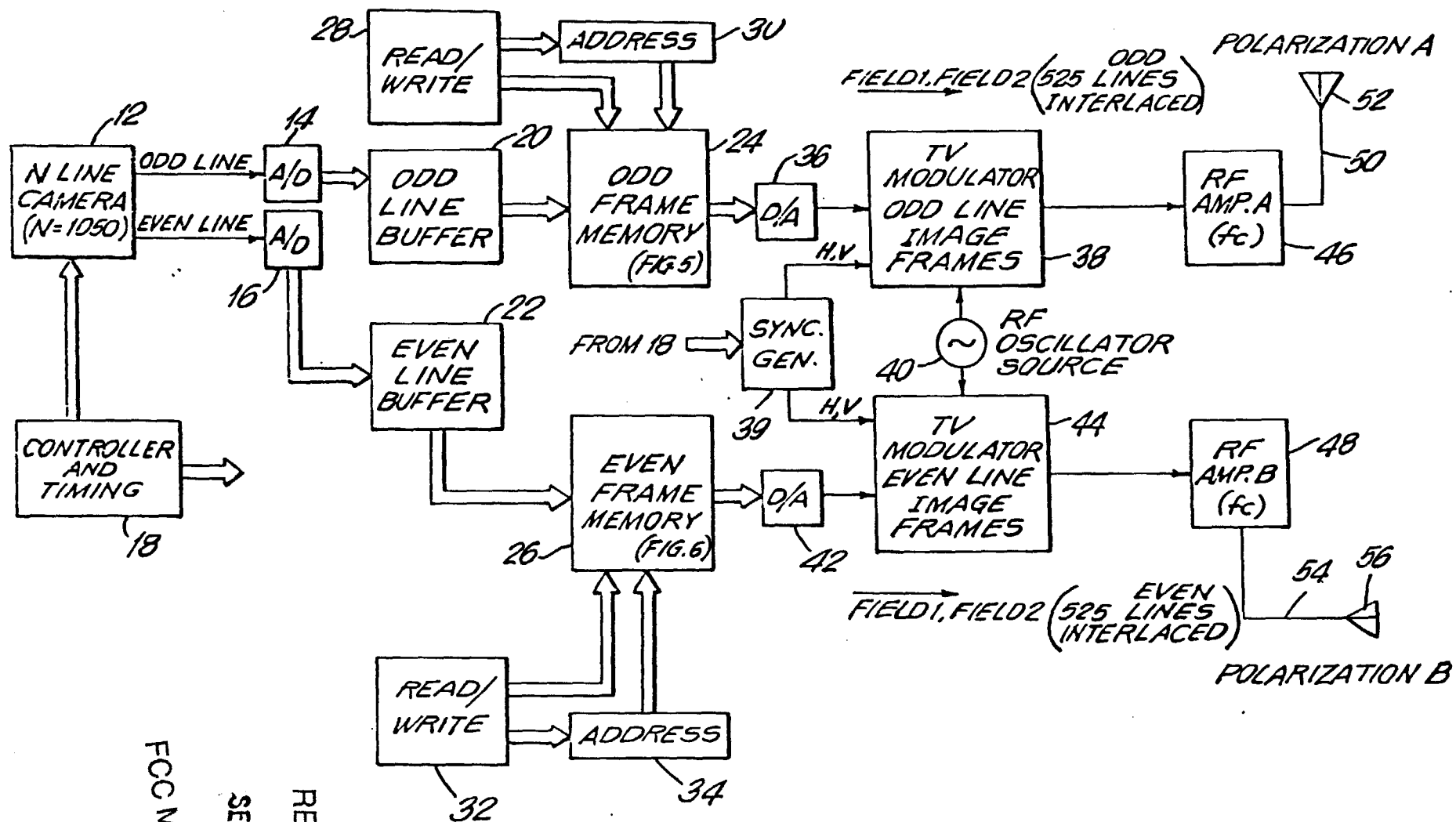


FIG. 1

FCC MAIL BRANCH

SEP 15 1991

RECEIVED

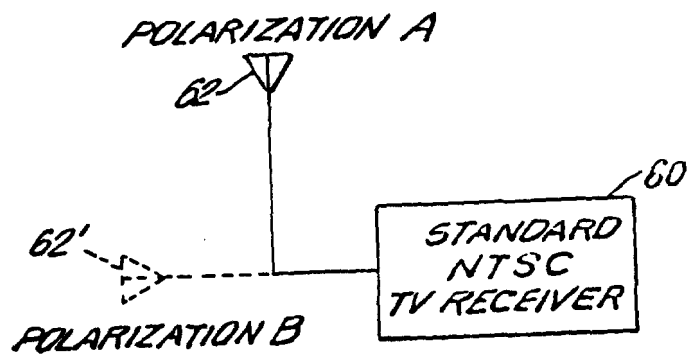
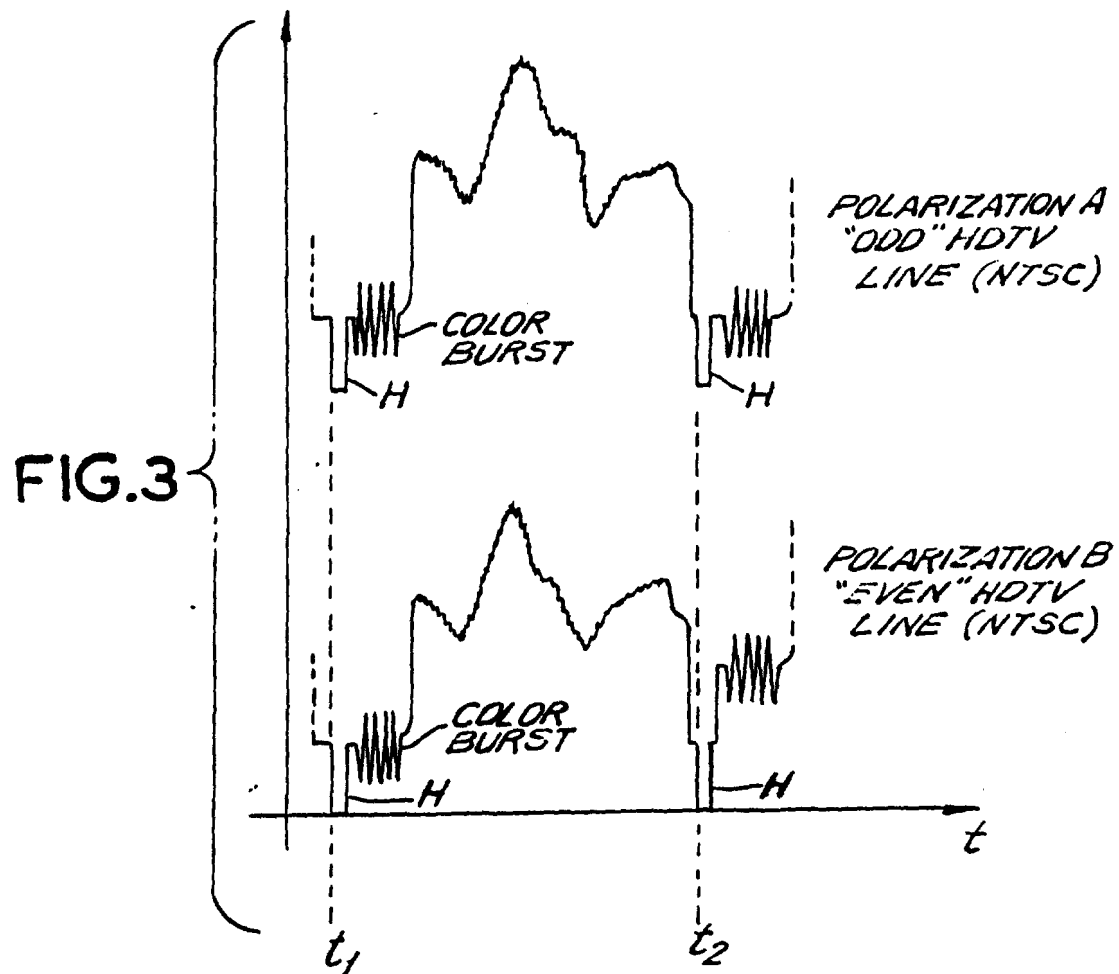


FIG.2



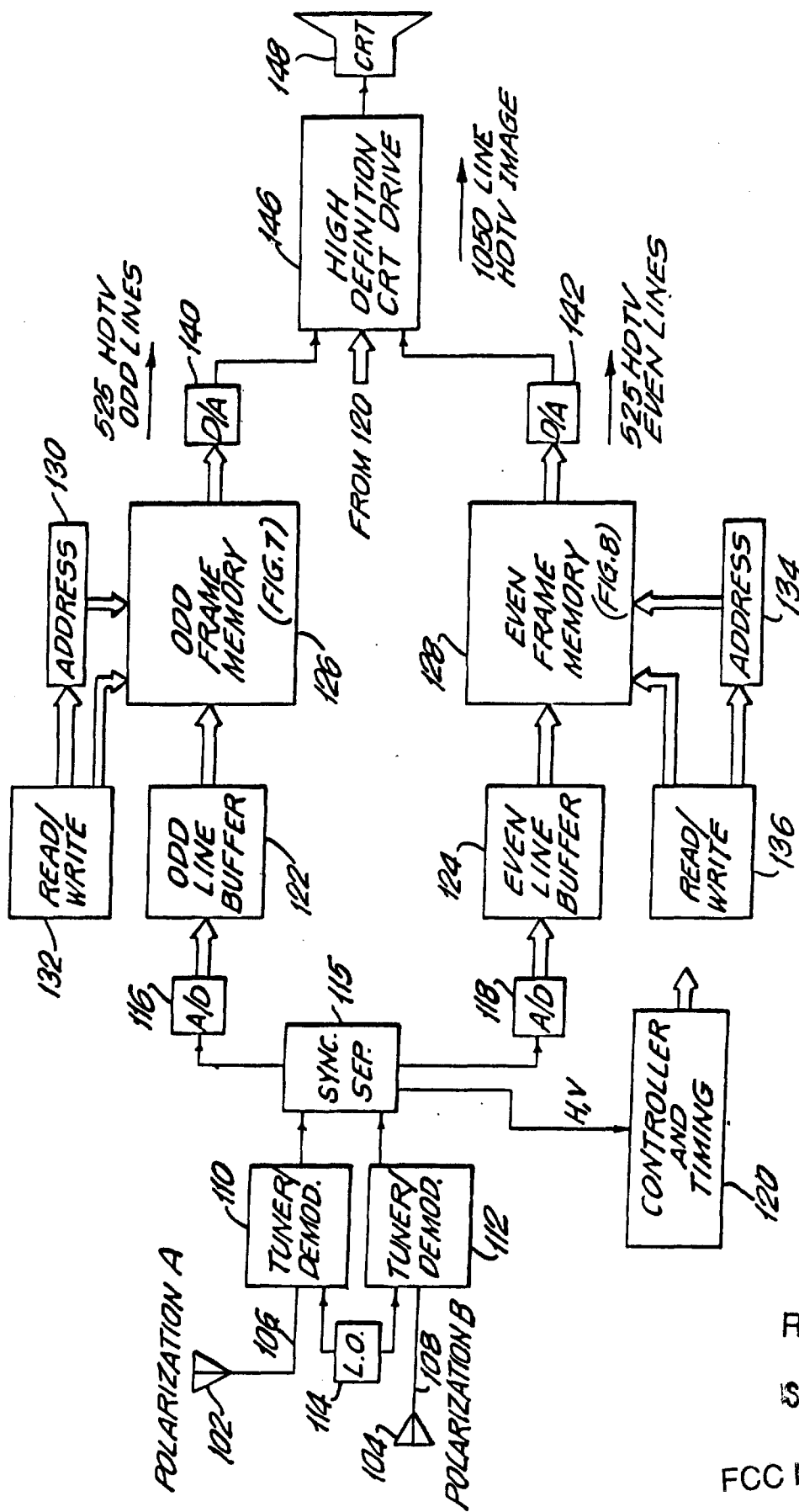


FIG. 4

RECEIVED

SEP 15 1980

FCC MAIL BRANCH

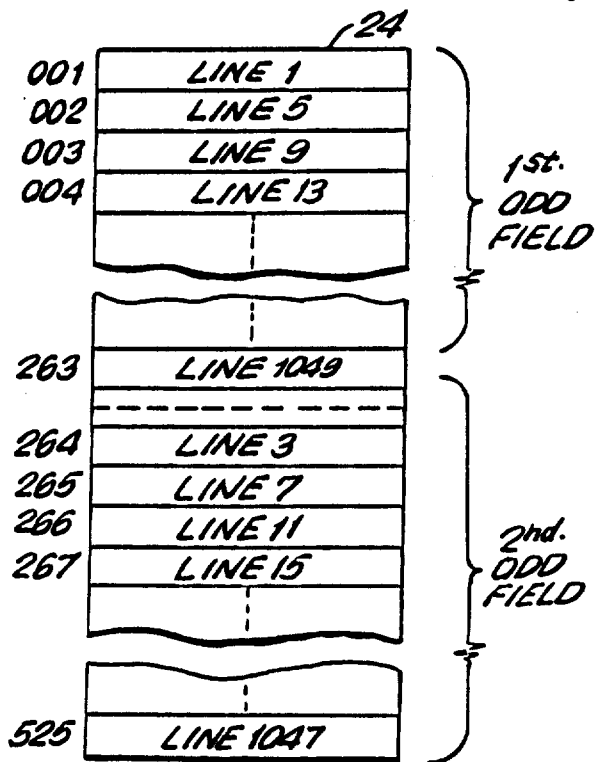


FIG. 5

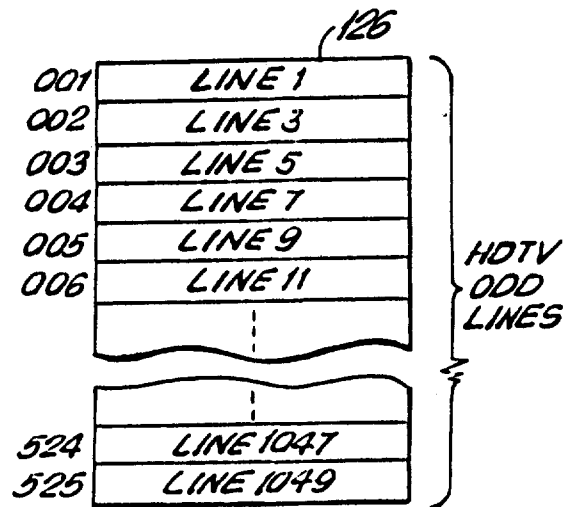


FIG. 7

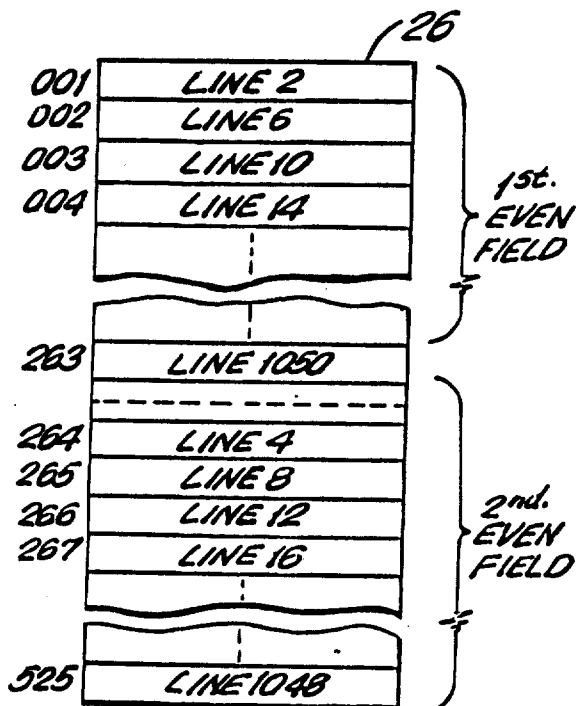


FIG. 6

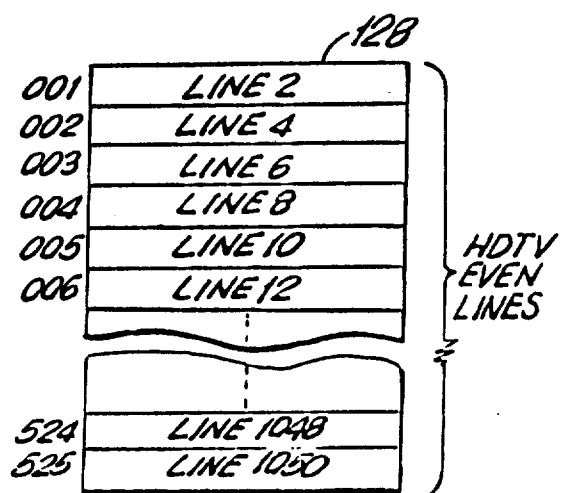


FIG. 8